Claim 1 (currently amended) A switch comprising:

a port card;

a network connected to the port card, the network having transmitters and receivers that communicate with each other and have assignments between each other;

a fabric connected to the port card through the network to send and receive stripes of fragments of packets to or from the port card, the port card, fabric and network having a plurality of modes of operation; and

a control mechanism connected to the transmitters and receivers which changes the assignments according to the mode, the control mechanism changing the mode and reusing the transmitters and receivers ~~where they can be reused~~.

Claim 2 (original): A switch as described in Claim 1 wherein the network is a gigabit network, the transmitters are gigabit transmitters and the receivers are gigabit receivers.

Claim 3 (original): A switch as described in Claim 2 wherein the network includes a mux structure that makes the assignments between transmitters and receivers.

Claim 4 (original): A switch as described in Claim 3 wherein the modes are 40G, 80G, 120G, 240G slow, 240G fast or 480G.

Claim 5 (original): A switch as described in Claim 4 wherein the network can support two modes simultaneously as combined modes.

Claim 6 (currently amended): A switch as described in Claim 5 wherein the combined modes are ~~40/80, 80/120, 120/160, 160/240 fast, 240 fast/240 slow, or 240 slow/480~~ 40G/80G, 80G/120G, 120G/160G, 160G/240G fast, 240G fast/240G slow, or 240G slow/480G.

Claim 7 (original): A switch as described in Claim 6 wherein each port card includes a striper and an unstriper.

Claim 8 (original): A switch as described in Claim 7 wherein the fabric includes a separator and an aggregator.

Claim 9 (currently amended): A switch as described in Claim 8 wherein the ~~assignments between~~ transmitters and receivers communicate with each other through the assignments at up to 1.3 GHz.

Claim 10 (original): A switch as described in Claim 9 wherein each transmitter takes in 8 bits of data and 2 bits of control and serially transmits the bits of data and control to the associated receiver.

Claim 11 (original): A switch as described in Claim 10 wherein each receiver recovers clock and data it receives by using an 8B/10B decoding protocol and provides 8 bits of data and 3 bits of control.

Claim 12 (currently amended): A method for switching fragments of packets comprising the steps of:

~~assigning~~ creating assignments between transmitters and receivers of a network;

changing a mode of [[the]] fabrics, port cards and networks;

changing the assignments of the transmitters and receivers according to the

mode and reusing the transmitters and receivers ~~where they can be reused~~; and

transferring the fragments of packets between fabrics and port cards with the

transmitters and receivers of the network.

Claim 13 (currently amended): A method as described in Claim 12 wherein the

changing the mode step includes the step of changing the mode no more than one step up or

down <u>in the mode sequence</u> at a time.

Claim 14 (canceled)

Claim 15 (currently amended): A method as described in Claim [[14]] <u>13</u>

wherein the changing the mode step includes the step of changing the mode between 40G and

80G, or 80G and 120G, or 120G and 160G or 160G and 240G slow or 240G slow 240G fast.

Claim 16 (currently amended): A method as described in Claim 15 wherein the

~~assigning~~ <u>creating</u> step includes the step of ~~assigning~~ <u>creating</u> assignments between the

receivers and transmitters to support two modes simultaneously as combined modes.

Claim 17 (original): A method as described in Claim 16 wherein the transferring step includes the step of transferring with the transmitter 8 bits of data and 2 bits of control serially through a mux structure to the receiver assigned to the transmitter.